In the Claims:

Claim 1 (currently amended): A memory ~~structure~~ transistor comprising:

a substrate having a drain region, a source region and a channel region, said channel region being between said source region and said drain region;

a gate layer formed over said channel region of said substrate;

a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays to pass through said tunable interlayer dielectric to said gate layer.

Claim 2 (currently amended): The memory ~~structure~~ transistor of claim 1, wherein said tunable material comprises a plurality of liquid crystal droplets, each of said plurality of liquid crystal droplets having a corresponding crystal director, said corresponding crystal director defining a polar orientation of each of said plurality of liquid crystal droplets.

Claim 3 (currently amended): The memory ~~structure~~ transistor of claim 2, wherein said corresponding crystal director has a random orientation within said matrix during said opaque state.

Claim 4 (currently amended): The memory ~~structure~~ transistor of claim 3, wherein said opaque state is enabled when an electric field is not applied across said tunable interlayer dielectric.

Claim 5 (currently amended): The memory ~~structure~~ transistor of claim 3, wherein said opaque state is enabled when a magnetic field is applied across said tunable interlayer dielectric.

Claim 6 (currently amended): The memory ~~structure~~ transistor of claim 2, wherein said corresponding crystal director has a uniform orientation within said matrix during said transparent state.

Claim 7 (currently amended): The memory ~~structure~~ transistor of claim 6, wherein said transparent state is enabled when an electric field is applied across said tunable interlayer dielectric.

Claim 8 (currently amended): The memory ~~structure~~ transistor of claim 6, wherein said transparent state is enabled when a magnetic field is not applied across said tunable interlayer dielectric.

Claim 9 (currently amended): The memory ~~structure~~ transistor of claim 1, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

Claim 10 (currently amended): The memory ~~structure~~ transistor of claim 1, wherein said matrix is polymer.

Claim 11 (currently amended): The memory ~~structure~~ transistor of claim 1, wherein said gate layer includes a charge storing layer.

Claims 12-21 (canceled).

Claim 22 (currently amended): A memory ~~structure~~ transistor comprising a substrate having a drain region, a source region and a channel region, said channel region being between said source region and said drain region, said memory ~~structure~~ transistor further comprising a gate layer formed over said channel region of said substrate, said gate layer including a charge storing layer, said memory ~~structure~~ transistor characterized by:

a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state

allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays from passing through said tunable interlayer dielectric to said gate layer.

Claim 23 (currently amended): The memory ~~structure~~ transistor of claim 22, wherein said tunable material comprises a plurality of liquid crystal droplets, each of said plurality of liquid crystal droplets having a corresponding crystal director, said corresponding crystal director defining a polar orientation of each of said plurality of liquid crystal droplets.

Claim 24 (currently amended): The memory ~~structure~~ transistor of claim 23, wherein, during said opaque state, said corresponding crystal director has a random orientation within said matrix.

Claim 25 (currently amended): The memory ~~structure~~ transistor of claim 23, wherein, during said transparent state, said corresponding crystal director has a uniform orientation within said matrix.

Claim 26 (currently amended): The memory ~~structure~~ transistor of claim 25, wherein said transparent state is enabled by providing an electric field through said tunable interlayer dielectric.

Claim 27 (currently amended): The memory ~~structure~~ transistor of claim 22, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

Claim 28 (currently amended): The memory ~~structure~~ transistor of claim 22, wherein said matrix is polymer.

Claim 29 (currently amended): The memory ~~structure~~ transistor of claim 22, wherein said gate layer includes a charge storing layer.